MOSFET Bulk Effect Behaviour and Estimation for Microwave-Frequency Modeling

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Abstract— **This paper describes MOSFET bulk effect behaviour as a function of width and gate/drain bias. The conductance from the intrinsic bulk to the bulk straps is measured directly using a modified MOSFET device. Measurements confirm that the bulk conductance follows a linear relation with respect to device width and is dependent on both gate and drain bias. By extracting the bulk conductance using low frequency S-parameter measurements, the paper presents a method to identify which MOSFET layout gives the lowest bias dependency on bulk effects. Due to active area edge effects, fairly small finger widths appear to greatly simplify bulk effect modeling for RF applications. The validity of extracted bulk effects are investigated at microwave frequencies by comparing device simulations with measurements.**

I. Introduction

In recent years, much research has been devoted to RF MOSFET modeling due to the potential of CMOS for fabrication of low-cost RFICs. As low-frequency MOSFET modeling is a well-established discipline, common microwave models consist of a low-frequency model for the intrinsic core embedded in a lumped parasitic network. The intrinsic model can either be an equivalent circuit [1] or a compact model such as BSIM3v3, EKV or MOS model 9 [2]. The extraction of MOSFET parasitics, in particular the bulk related parasitics, is often problematic due to the four-terminal nature of the MOSFET. For measurements of MOSFETs in the common-source configuration, bulk parasitics can be hard to separate from intrinsic parasitics. Bulk effects can be estimated using a number of methods, including optimization [1], 2D simulations [3], or direct measurements [4].

The objective with this paper is to analyze bulk parasitics, the bulk conductance in particular. In order to obtain the best possible accuracy for the bulk conductance estimate, the measurement approach has been chosen. The behaviour of the bulk conductance at microwave frequencies is investigated, focusing on the bulk conductance dependence on MOSFET width and gate/drain bias. The validity of the extracted bulk conductance is verified by comparing measured MOSFET output characteristics with simulations, including and excluding the effect of the extracted bulk conductance on the simulated response.

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II. Bulk Effect Analysis

A. Layout Methodology and Bulk Conductance

In [5], the work needed to extract parasitics for any number of MOSFETs is reduced by sacrificing a small amount of layout flexibility. The layout methodology is to let each transistor be a parallel combination of one or more unit transistors. This unit transistor is called a *cluster of fingers* (COF). For MOSFETs laid out using COFs, only one structure has to be modeled and the resulting parasitics are then found by parallel combinations of the COF parasitics. As excellent parasitic scalability has been obtained using this method, in particular with regards to bulk conductance [5], this method forms the basis for the MOSFET test structures fabricated in conjunction with this work. An MOSFET COF is shown in Fig. 1a.

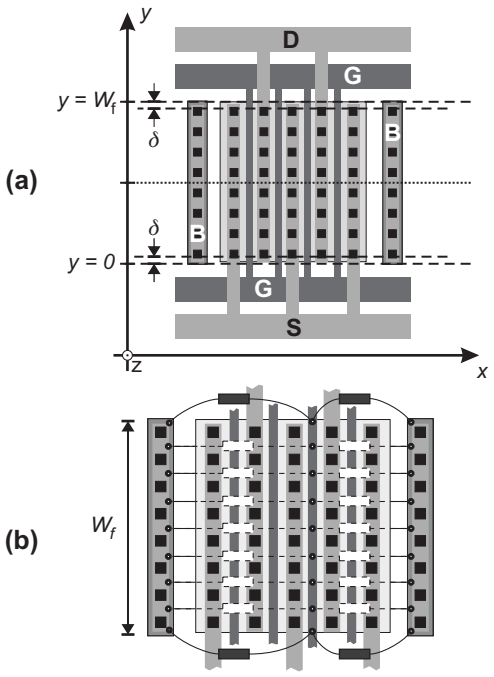

Fig. 1. **(a)** An MOSFET COF. The dotted line indicates active area symmetry and the dashed lines denote the areas dependent on edge geometry. **(b)** Bulk conductance distribution in an MOSFET COF. Some interconnects are omitted for clarity.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

Bulk conductance, $G_{b,T}$, is the conductance from the intrinsic bulk (substrate surface located immediately below the gate) to the accessible bulk (bulk straps outside the active area). This conductance has a significant impact on the MOSFET output characteristics at microwave frequencies [6]. Due to the distributed nature of the bulk conductance, it can be modeled using a network of linear resistors [6]. Fig. 2 shows the simplest bulk resistor network, which is a single linear resistor connected from the model's intrinsic bulk terminal (B') to the external bulk terminal (B). As this model has been proven valid to 10 GHz using BSIM3v3 simulations [3], the present analysis of the measured bulk conductance is based on this model.

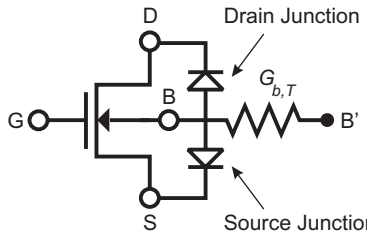

Fig. 2. An intrinsic MOSFET model and bulk related parasitics.

B. Width and Bias Dependence

To determine the influence of geometry on the bulk conductance, the bulk conductance for a single finger of the COF structure, G_b, is analyzed. This conductance is measured from the intrinsic bulk below the entire length of the finger to the accessible bulk straps on either side of the COF. The intrinsic bulk below the gate finger is divided into a number of infinitesimal areas along the *y*-axis, and the individual contributions, denoted $g_b(y)$, are examined.

The structure in Fig. 1 is symmetric about $y = W_f/2$. At a minimum distance δ from the edges of the active area, all cross sections taken parallel to the *xz*-plane are identical and $g_b(y)$ is independent of the geometry around the edges of the active area. This implies that

$$g_b(y) = g_w; \quad y \in [\delta, W_f - \delta] \tag{1}$$

where g_w is constant with respect to y. This means that $g_b(y)$ can be divided into constant contributions from the inside of the MOSFET (the white components in Fig. 1b) and contributions depending the geometry around the edges of the active area (the black components in Fig. 1b). The total bulk conductance for the finger is found by integrating Eq. (1), i.e.

$$G_b = \int_0^{W_f} g_b(y)dy = g_w W_f + G_0 \tag{2}$$

where

$$G_0 = -2\delta g_w + 2\int_0^{\delta} g_b(y)dy \tag{3}$$

is independent of W_f. This means that the bulk conductance should scale linearly with W_f apart from a constant term dependent on the edge geometry. Bias voltages affect the bulk conductance in at least two ways:
Depletion effect: As bias is applied to the drain (or source), the depletion areas move deeper into the epitaxial layer forcing the current to take a longer route from the intrinsic bulk to the bulk straps. This decreases the bulk conductance
Gate effect: As the gate voltage is increased, electrons are pulled towards the oxide layer leaving additional holes (positive ions) in the bulk, increasing the effective conductivity of the substrate.

III. Measurements

The cluster of fingers used for verification of the bulk conductance measurements corresponds to the one shown in Fig. 1. The COF consists of four double-contacted gate fingers with a finger width of 5 μm laid out with symmetric bulk contacts. The structures were fabricated in a 0.25 μm technology.

A. Test Structures

In order to be able to measure the conductance from the intrinsic bulk to the accessible bulk directly, the COF must be modified to provide a direct connection to the silicon placed immediately below the gate. This is done by replacing one of the gates with bulk contacts, as shown in Fig. 3 [4]. This structure is then mounted in a shield-based test fixture with source and bulk nodes grounded. The gate replacement is connected to a GSG signal pad. A single DC pad is connected to the remaining gates and the drain areas, denoted V_b in Fig. 3

To obtain g_w, a total of three test structures of different finger widths have been produced (3, 10 and 20 μm finger width). The measured conductance is the total bulk conductance for one finger and must be adjusted accordingly when estimating the bulk conductance for the entire COF. Replacing the gate with a bulk strap does not result in an identical structure, as the p+ diffusion in the bulk strap has a different conductivity than the epitaxial layer. As the conductivity of the epitaxial layer is low, this error is not expected to significantly affect the results.

B. Measurement Method and Parameter Extraction

The test structures were measured on-chip from 45 MHz to 18 GHz using an HP8510C *vector network analyzer* (VNA). The VNA was calibrated and the resulting measurements were de-embedded to remove the influence of pads and leads. The gate/drain voltage, V_b, was stepped from 0.00 V to 2.50 V in 0.25 V steps for all three finger widths. The bulk conductance for a single finger, G_b, was estimated as

$$G_b \approx \Re\{Y_{in}(f)\}|_{f=45\text{ MHz}} \tag{4}$$

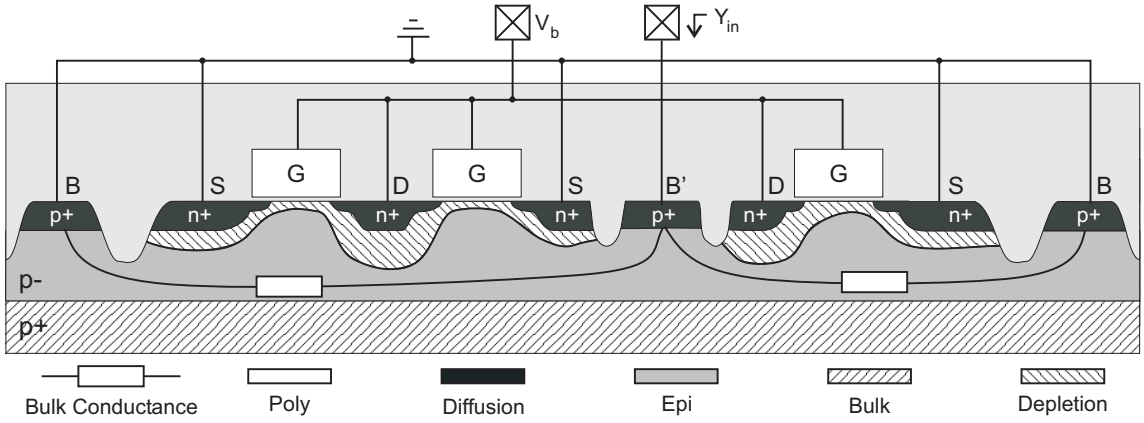

Fig. 3. A cross-section of a modified MOSFET COF used for the bulk conductance measurements. The voltage V_b is the gate and drain bias voltage and Y_{in} is the conductance from the intrinsic to the accessible bulk.

where $Y_{in}(f)$ is found by S- to Y-parameter conversion of the measured data. The parameters G_0 and g_w were found for each bias point by fitting G_b to Eq. (2) using the least-squares method. The total output conductance, $G_{b,T}$, for a MOSFET laid out using a COF with N_f fingers and a finger width of W_f is roughly estimated as the parallel combination of the bulk conductance for an individual COF, i.e.

$$G_{b,T} \approx N_f N_c (g_w W_f + G_0) \tag{5}$$

where N_c is the number of COFs in the transistor.

IV. Results

The measured conductance as a function of W_f, including the linear fit, is shown in Fig. 4. The values extracted at 45 MHz were verified using low-voltage DC-conductance measurements. The difference between the conductance values extracted at RF and DC was below 2.3% for all finger widths, which implies that the extracted values for G_b are valid. The extracted parameters G_0 and g_w are shown versus bias voltage in Fig. 5.

The width scaling parameter, g_w, first increases slightly, then decreases with increasing bias voltage. The parameter G_0 behaves in the opposite way, first decreasing slightly and then increasing as the bias voltage is increased. A possible explanation is, that by applying a bias voltage to the gate, electrons are attracted to the channel increasing the conductivity of the epitaxial layer. Increasing drain bias counteracts this, eventually blocking off the areas with increased conductivity and forcing the currents to take a longer route from the intrinsic bulk to the bulk straps, dominating the bulk conductance at higher bias voltages. Although the same effects are at work for G_0, the differences in the geometry outside the active area result in a different bias dependency. As the *field oxide* (FOX) layer over the bulk next to the active area is thicker than the gate oxide, it takes a larger voltage to increase the conductivity. The depletion area plays a similar role for G_0, but as its extension into the bulk is limited by the small thickness of the diffusion areas, the effect is not as great as for g_w.

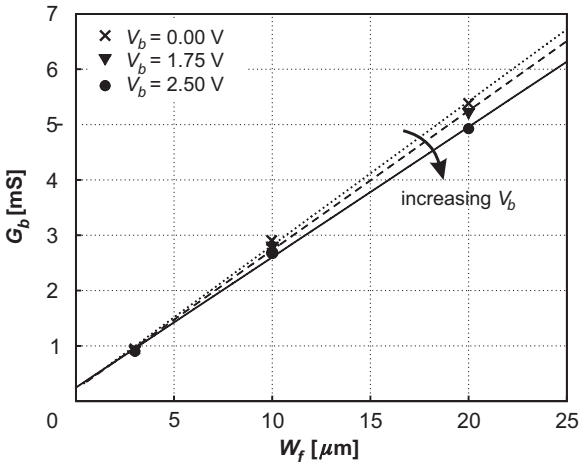

Fig. 4. The measured bulk conductance as a function of transistor width. The dotted, dashed, and solid lines are linear fits of the data sets.

As the incremental changes in g_w and G_0 have opposite signs over the bias range, choosing the appropriate width can minimize the bias variation in conductance. The maximum conductance spread over the bias range, $\Delta_{max}(W_f)$, is found using:

$$\Delta_{max}(W_f) = \frac{\max(G_b(W_f, V_b))}{\min(G_b(W_f, V_b))} - 1 \tag{6}$$

which is plotted versus finger width in Fig. 6.

In order to investigate the validity of the extracted bulk conductance parameters, measurements of a 280×0.25 μm MOSFET biased in saturation have been compared to an equivalent model [1] including and excluding the effects of the bulk resistance. As the MOSFET is made up of 14 COFs

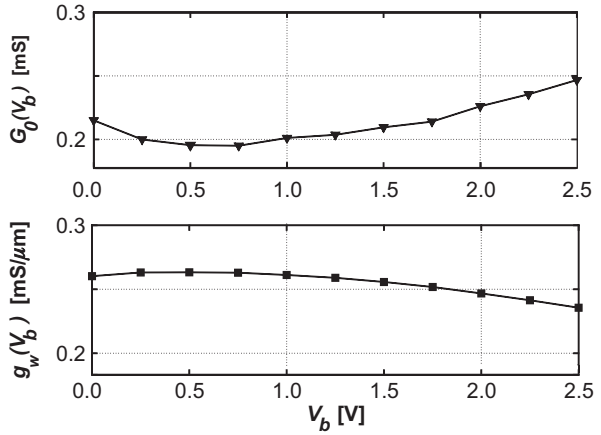

Fig. 5. Extracted values of g_w and G_0 versus drain/gate bias voltage, V_b.

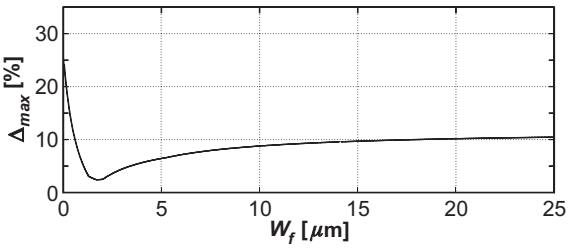

Fig. 6. Maximum relative variation, Δ_{max} versus W_f.

having 5 μm fingers, the output resistance ($G_{b,T}^{-1}$) is found to be 11.8 Ω. Although the transistor is biased with different voltages on the drain and source, i.e. 0.6 V on the gate and 1.0 V on the drain, the variation in the bulk conductance parameters for these voltages is minimal, as can be seen from Fig. 5.

The output reflection parameter s_{22} for both measurement and simulations is shown in Fig. 7. From this figure it is seen that the bulk conductance affects only the amplitude of the output reflection, not the phase. The simulations reveal that by assuming that the bulk conductance is identical for all four fingers and using the bulk conductance of one of the inner fingers, the bulk conductance is underestimated. By optimizing the bulk conductance to fit measurements, the best fit was obtained for $G_{b,T}^{-1} = 5\Omega$. This error can most likely be attributed to the difference in conductance between the two outer fingers and the inner fingers. This difference is due to less distance between the intrinsic bulk and the bulk straps and less influence from depletion areas, as there is only one source finger between the bulk straps and the intrinsic bulk.

V. Conclusions

By measuring modified COF test structures of different lengths for a series of bias points, the dependence of bulk

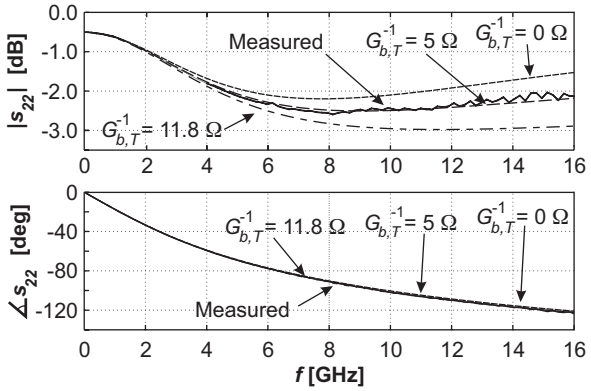

Fig. 7. Measurements of a 280×0.25 μm MOSFET in saturation (V_g = 0.6 V, V_d = 1.0 V) compared to simulations.

conductance on bias and finger length has been investigated. Due to consistent device layout, the bulk conductance scales linearly with finger width. The bulk conductance variations due to bias also behave according to expectation. The relative variation of bulk conductance over the bias range has been shown to be dependent on finger width. The variation has a minimum for a certain finger width, which means that the COF can be designed for minimum bias dependency of the bulk conductance.

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